

OBJECTION TO PREVIOUS AMENDMENT

The objection to the amendment filed April 24, 2000 under 35 U.S.C. § 132 as introducing new matter into the specification is respectfully traversed and should be withdrawn.

The characterization of the amendment filed April 24, 2000 as adding new matter to the specification is not correct.

"The proper basis for rejection of a claim amended to recite elements thought to be without support in the original disclosure . . . is §112, first paragraph, **not §132**. The latter section prohibits addition of new matter to the original disclosure. **It [§132] is properly employed as a basis for objection to amendments to the abstract, specifications, or drawings** attempting to add new disclosure to that originally presented." *In re Rasmussen*, 211 USPQ 323, 326 (C.C.P.A. 1981) (emphasis added by Applicants' representative).

The amendment filed April 24, 2000, amended only the claims. The basis of the objection is the amendments to claims 3 and 4 (page 3, lines 1-6, of the Office Action). Therefore, the objection under 35 U.S.C. § 132 is not proper and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112, FIRST PARAGRAPH

The rejection of claims 3 and 4 under 35 U.S.C. §112, first paragraph is respectfully traversed and should be withdrawn.

It is a well-known and long-accepted practice and principle in patent law that one need not describe every last

detail of an invention, else patent specifications would turn into production specifications which they were never intended to be (See *In re Gay*, 309 F.2d 769, 135 USPQ 311, 316 (C.C.P.A. 1962). To comply with the description requirement of 35 U.S.C. 112, first paragraph "all that is required is that the application reasonably convey to persons skilled in the art that, as of the filing date thereof, the inventor had possession of the subject matter later claimed by him" (*Forssmann v. Matsuo*, 23 USPQ 2d 1548, 1550 (B.P.A.I. 1992), *aff'd*, 991 F.2d 809 (Fed. Cir. 1993)).

FIG. 3 of the present application discloses an example of a programmable logic circuit. A person of ordinary skill in the art of programmable logic devices would know that the logic blocks of FIG. 3 could contain a look-up table or a product term array. For example, U.S. Patent No. 5,757,207 discloses logic blocks with product term based and look-up table based logic elements.

Furthermore, one skilled in the art would be able to make and/or use the presently claimed invention without undue experimentation, in light of the specification as originally filed. Therefore, the presently pending invention is fully described and enabled within the meaning of 35 U.S.C. § 112, first paragraph. As such, the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112, SECOND PARAGRAPH

The rejection of claims 5, 7-9, and 22-24 under 35 U.S.C. §112, second paragraph has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102(e)

The rejection of presently pending claims 2, 6, 10, 12, 15-16, 18, and 20-23 under 35 U.S.C. § 102(e) as being anticipated by Chou et al. is respectfully traversed and should be withdrawn. The rejection of presently pending claims 22-23 under 35 U.S.C. § 102(e) as being anticipated by Weiss et al. has been obviated by appropriate amendment and should be withdrawn.

Chou et al. disclose a clock synthesizer for low EMI applications (Title). The Office Action mischaracterizes the disclosure of Chou et al. (page 4, lines 4-17, of the Office Action). Chou et al. discloses that the synthesizer consists of a digital phase lock loop (DPLL) circuit (elements 1, 2, 3, 4, 6, and 9), a programmable logic array (PLA) 8, and a counter 10 (FIGS. 1 and 5, and column 1, lines 15-27). The PLA 8 only has inputs SEL0 and SEL1 which correspond with four different binary values (column 2, lines 4-6, of Chou et al.). The inputs are used to select dividing numbers (column 2, lines 9-11, of Chou et al.). Thus, the PLA 8 receives no clock signals as inputs.

In contrast, the presently claimed invention provides a programmable logic circuit that may be configured to (i) generate one or more control signals and (ii) **receive one or more clock signals**. Assuming *arguendo*, that the PLA 8 of Chou et al. is similar to the presently claimed programmable logic circuit (a presumption with which Applicants' representative does not necessarily agree), where are the one or more clock signals? Chou et al. fail to disclose a programmable logic circuit configured to **receive one or more clock signals**. Therefore, Chou et al. do not disclose or suggest all the elements of the presently claimed invention. As such, the presently pending claims are fully patentable over the cited reference and the rejection should be withdrawn.

Weiss et al. disclose a data processing system having a register controllable speed (Title). FIG. 4 of Weiss et al. shows a clock input **divided** into a number of clocks by the dividers block 404. Binary data stored in registers is used by a 4-to-16 line decoder to **select** one of the number of clocks (FIGS. 4 and 5, and column 1, lines 43-49, of Weiss et al.). The clock signals of Weiss et al. are **not** generated in response to a reference clock **and one or more control signals**.

Weiss et al. do not disclose or suggest either (i) a **means for implementing programmable logic** for manipulating information to generate one or more control signals, where the

means for implementing programmable logic receives one or more clock signals or (ii) **a means for generating** the one or more clock signals in response to a reference clock **and** the one or more control signals, as presently claimed. Furthermore, Weiss et al. do not disclose or suggest means for implementing programmable logic and means for generating are integrated on a single circuit, as is presently claimed. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

**CLAIM REJECTIONS UNDER 35 U.S.C. §103**

The rejection of claims 7-9, and 19 as being unpatentable over Chou et al. in view of Davis et al. and claims 5, 17, and 24 as being unpatentable over Chou et al. in view of Appel is respectfully traversed and should be withdrawn. Claims 5, 7-9, 17, 19, and 24 depend, either directly or indirectly, from the independent claims 12, 15, and 22, which are believed to be fully patentable. As such, the presently pending claims are fully patentable over the cited reference and the rejection should be withdrawn.

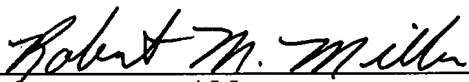
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 02-2712.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

  
\_\_\_\_\_  
Robert M. Miller  
Registration No. 42,892  
24025 Greater Mack, Suite 200  
St. Clair Shores, MI 48080  
(810) 498-0670

Dated: September 27, 2000

Docket No.: 0325.00063